ABSTRACT OF THE DISCLOSURE

A nonvolatile memory apparatus including a control circuit, plural terminals including clock, command and other terminals, a clock generator, and plural nonvolatile memory cells. The clock and command terminals respectively receive a first clock signal and commands including read and program commands. The clock generator generates a second clock signal. In response to the read command, the control circuit controls reading data from the memory cells, and outputting data via the other terminal not the command terminal in response to the first clock signal. In response to the program command, the control circuit controls receiving data via the other terminal not the command terminal in response to the first clock signal, and writing data to the memory cells. The data writing to ones of said nonvolatile memory cells is performed using the second clock signal.